FPGA Based Implementation and Comparison of Beamformers for CDMA2000

Sener Dikmese · Adnan Kavak · Kerem Kucuk · Suhap Sahin · Ali Tangel

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Abstract For the integration of smart antennas into third generation code division multiple access (CDMA) base stations, it still remains as a challenging task to implement smart antenna algorithms on programmable processors. In this paper, we study implementations of some CDMA compatible beamforming algorithms, namely least mean square (LMS), constant modulus (CM), and space code correlator (SCC) algorithms, using Xilinx’s Virtex family FPGAs. This study exhibits feasibility of implementing even simple, practical, and computationally small algorithms based on today’s most powerful FPGA technologies. 16 and 32 bits floating point implementations of the algorithms are investigated using both Virtex II and Virtex IV FPGAs. CDMA2000 reverse link baseband signal format is used in the signal modeling. Randomly changing fading and Direction-of-arrivals (DOAs) of multipaths are considered as a channel condition. The implementation results in terms of beamforming
accuracy, FPGA resource utilization, weight vector computation time, and DOA estimation error are presented. Beamformer weight vectors using LMS and CM can be computed within less than 20 µs on Virtex II FPGA and 10 µs on Virtex IV FPGA, and using SCC it can be achieved within less than 22 µs on Virtex IV FPGA. These results show that FPGAs provide approximately 500 times faster speed in implementations than our previous work with DSPs.

**Keywords**  Adaptive algorithms · CDMA2000 · FPGA · DSP · DOA estimation · Smart antenna system (SAS) · Software radio · 3G systems

1 Introduction

Software defined radio (SDR) is generally defined as a radio with software functionality, which requires programmable processors to perform the signal processing necessary to transmit and receive baseband information at radio frequency [1,2]. Since the radio functionalities can be updated very effectively by software, this technology provides greater flexibility in the implementation of systems. For 3G wireless systems, SAS is a technology that provides improved system capacity and spectral efficiency. One of the difficulties adapting a SAS into 3G CDMA base station is the implementation of algorithms on programmable processors. SDR implementation of beamforming algorithms on programmable processors such as digital signal processors (DSPs), field programmable gate array (FPGAs), or special type of application-specific integrated circuits (ASICs) is a key point for upgrading existing 3G base stations. FPGAs with their re-programmable logic gates and functions are hardware oriented devices that can be preferred for time critical applications requiring high processing speed [3]. Compared to FPGAs, other alternative processors such as DSPs are more flexible and reprogrammable devices which are widely used in signal processing applications [4].

Various wireless standards in 2G and 3G systems with different access techniques (FDMA, TDMA, CDMA, WCDMA, Cdma2000) and modulation schemes need the investigation of smart antenna processing schemes that can be software-implementable in programmable processors. With the emergence of 3G wireless systems, many research efforts have been focused on the development of beamforming algorithms for CDMA systems [5,6].

There have been some studies regarding the implementation of smart antenna algorithms using programmable processors. Normalized constant modulus algorithm (NCMA) was implemented in [7] using Xilinx’s SPARTAN II FPGA to demonstrate digital beamforming capability of an FPGA. In [8], using TI’s C6711 DSP for beamformer weight vector estimation in cdma2000 was introduced. Optimal weight vector in C6711 DSP was computed such that maximization of the signal to interference plus noise ratio (SINR) by using Lagrange’s formula for generalized eigenvector solution is utilized. Im and Choi [9] demonstrated a smart antenna implementation where C6701 based beamformer using Lagrange’s formula for generalized eigenvector solution is used for Korean CDMA WLL. In a very earlier work, Choi et al Linearized Conjugate Gradient Method (LCGM) implemented beamforming on a general-purpose DSP with a clock frequency of 30 MHz In [10], a software radio based smart antenna base station was developed for GSM/DSC system by Siemens ICN consisting of an 8-element antenna array, 8 TI’s C6701 DSP processors, and 8 co-processors implemented in Xilinx’s XCV400E FPGA technology. In [11], using LMS and Recursive Least Squares (RLS) algorithms, a DSP based implementation on TI’s C6211 processors of reverse link beamformers for a Wideband Code Division Multiple Access (WCDMA) was shown. Dynamic channel conditions in which multipath fading coefficients and DOAs change randomly were not considered in [11] for the performance of the