Leakage Current Optimization Techniques During Test Based on Don’t Care Bits Assignment

Wei Wang¹,² (王伟), Yu Hu² (胡瑜), Yin-He Han² (韩银和), Xiao-Wei Li³ (李晓维)
and You-Sheng Zhang¹ (张佑生)

¹School of Computer and Information, Hefei University of Technology, Hefei 230009, China
²Key Laboratory of Computer System and Architecture, Institute of Computing Technology, Chinese Academy of Sciences
³Beijing 100080, China

E-mail: {wang_wei, hu_yu, yinhe, lxiw}@ict.ac.cn; zhangyss@mail.hf.ah.cn
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Abstract It is a well-known fact that test power consumption may exceed that during functional operation. Leakage power dissipation caused by leakage current in Complementary Metal-Oxide-Semiconductor (CMOS) circuits during test has become a significant part of the total power dissipation. Hence, it is important to reduce leakage power to prolong battery life in portable systems which employ periodic self-test, to increase test reliability and to reduce test cost. This paper analyzes leakage current and presents a kind of leakage current simulator based on the transistor stacking effect. Using it, we propose techniques based on don’t care bits (denoted by Xs) in test vectors to optimize leakage current in integrated circuit (IC) test by genetic algorithm. The techniques identify a set of don’t care inputs in given test vectors and reassign specified logic values to the X inputs by the genetic algorithm to get minimum leakage vector (MLV). Experimental results indicate that the techniques can effectively optimize leakage current of combinational circuits and sequential circuits during test while maintaining high fault coverage.

Keywords leakage current, don’t care bits, minimum leakage vector, leakage power

1 Introduction

It is well known that power dissipation during test mode can be significantly higher than that during functional mode. Sometimes, the test power could be twice as high as the power consumed during the normal mode. Furthermore, the proportion of the leakage current power to the total power increases rapidly. Consequently, as leakage current becomes a big contributor to test power consumption, leakage current optimization in test will be a very important research topic. In recent years, dynamic power consumption is a dominant component of total power dissipation during test. A considerable amount of effort has been expended in reducing dynamic power or other test cost. However, as technology scales down below 0.13 micron, the absolute and the relative contribution of leakage power to the total system power during test is expected to further increase because of the exponential increase in leakage current, setting leakage power consumption on the path to dominating the total power used by the CPU. Thus, reducing leakage current during test is also becoming an increasingly important issue. Especially to Very Deep Sub-Micron (VDSM) IC (integrated circuit) during test, large leakage current would cause crosstalk noise and functional failures etc. Sometimes, the signal distortion gets so worse that there is much misdetection. In addition, large leakage power in test generates lots of heat dissipation which may lower transistors’ reliability, and even cause physical damage to transistors. Hence, in order to increase test reliability and lower negative effect on circuits under test, the leakage current should be well under control during test.

In current VDSM technology era, the researches on leakage current during test are in its gestation phase, and there are some leakage reduction techniques using low-power design methodologies. One of the techniques is Input Vector Control — during standby mode the power management units drive the circuit inputs to a pre-computed MLV (minimum leakage vector). Power Gating is a good way to reduce leakage current and dynamic power. However, it is difficult to design the Power Gating because of...
a trade-off between area, power and performance. It also takes too much area overhead so that it is seldom used in practice. Other methodologies such as Threshold Voltage Control and Source Biasing could reduce IC’s (integrated circuit) leakage current caused by sub-threshold leakage current to a certain extent, but it would lower performance as a sacrifice at the same time[6,20-22].

In this paper, using characteristics of test, we propose techniques based on don’t care bits assignment to optimize the leakage current when combinational or sequential circuits are under test. This paper is organized as follows. Section 2 describes the constituents of the leakage current, the transistor stacking effect and the leakage current simulator. Section 3 provides the optimization techniques which are based on don’t care bits assignment using the genetic algorithm, and applies the techniques to combinational circuits and sequential circuits during test. In Section 4, we present simulation results of the techniques and compare them with related work. Finally, we conclude in Section 5.

2 Leakage Current Analysis and Estimation

2.1 Leakage Current Analysis

In order to effectively reduce leakage current during test, firstly we should estimate the leakage current which is composed of sub-threshold leakage current, gate-oxide leakage current and band-to-band-Tunneling leakage[23]. In current CMOS (Complementary Metal-Oxide-Semiconductor) technologies, the sub-threshold leakage current is much larger than other leakage current components. So we focus on estimating the sub-threshold current instead of the total leakage current. The sub-threshold current is the drain-source current of an OFF transistor and it can be calculated by the following equation[24]:

\[ I_{\text{sub}} = \mu_0 \frac{w_{\text{eff}}}{L_{\text{eff}}} \left( \frac{q}{2} \Phi \right)^{\frac{1}{2}} \exp \left( \frac{Q_\text{eff} N_{\text{eff}}}{2 q} \left( 1 - e^{-\frac{V_{\text{gs}}}{kT}} \right) \right) \]

where \( \mu_0 \) is the zero bias mobility and \( \gamma \) is the linear body effect coefficient. \( \eta \) is the drain-induced barrier lowering (DBL) coefficient, representing the effect of \( V_{\text{ds}} \) on threshold voltage. Here, \( L_{\text{eff}}, W_{\text{eff}} \) and \( V_T \) present the effective channel length, the effective width and the thermal voltage, respectively. For a small individual device, leakage current can be calculated by (1). But for a whole circuit, the leakage current cannot be computed by (1) because of the high time complexity etc. Therefore, how to estimate VLSI circuit’s leakage current quickly and effectually is an important problem to be explored.

In fact, the stacking effect, which is caused by the transistor body effect, can have an impact on the sub-threshold current to a certain extent. Turning “OFF” more than one transistor in a stack of transistors forces the intermediate node voltage to go to a value higher than zero, which causes a negative \( V_{\text{gs}} \), negative \( V_{\text{ds}} \) (more body effect) and reduces \( V_{\text{ds}} \) (less DBL) in the top transistor, thereby considerably decreasing the sub-threshold current flowing through the stack. This effect, known as the “stacking effect”[23], has been widely used to reduce the sub-threshold leakage in logic circuits. The current drawn by the logic block is dependent on the configuration of the ON and OFF transistors. The OFF transistors draw the leakage current while the ON transistors provide the conducting paths to the power supply nodes[26]. So the leakage current of a circuit depends on its input vectors combination, and we can reduce leakage current in CMOS VLSI circuits by input test vectors control.

2.2 Leakage Current Estimation

Most existing leakage estimation models are based on circuit level and have a high time complexity. Therefore, better leakage estimation method should be created in the advanced technology era[27].

<table>
<thead>
<tr>
<th>Input Vector</th>
<th>Output</th>
<th>Leakage Current (( \mu A ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>011</td>
<td>0</td>
<td>2599.40</td>
</tr>
<tr>
<td>110</td>
<td>1</td>
<td>155.50</td>
</tr>
<tr>
<td>101</td>
<td>1</td>
<td>158.77</td>
</tr>
<tr>
<td>011</td>
<td>1</td>
<td>173.35</td>
</tr>
<tr>
<td>001. 100. 010</td>
<td>1</td>
<td>31.4575</td>
</tr>
<tr>
<td>000</td>
<td>1</td>
<td>18.0386</td>
</tr>
</tbody>
</table>

Because of the stacking effect, the leakage of a circuit depends on its input vectors. Table 1 shows different leakage current values for all input combinations of a 3-input NAND gate. When the input combinations are 001, 100 and 010, they cause approximate values of leakage current. To simplify, we regard them as the same values. This phenomena caused by the stacking effect, also occurs in other kinds of logic gates. Based on the phenomena, a kind of leakage current simulator is built up to estimate the leakage current.

The following procedure describes how the simulator can be used to calculate the leakage current of a CMOS circuit during test.

1) Build the models of all kinds of logic gates using the BPTM (Berkeley Predictive Technology Model). Because it is seldom that logic gates have more than 10 inputs in CUT, we can simplify the problem. For example, we only consider from 2-input NAND gate to 10-input NAND gate.