Effects of the Gold Thickness of the Surface Finish on the Interfacial Reactions in Flip-Chip Solder Joints

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The effects of Au thickness on the flip-chip solder joints with Cu/Ni/Al under-bump metallurgy (UBM) on one end and the Au/Ni surface finish on another was studied. Two different thicknesses, 0.1 µm and 0.65 µm, were used for the surface finish. After assembly, the joints were subjected to thermal aging at 150°C. The difference in Au thickness had a strong effect on the consumption rate of the Ni layer in the UBM as well as on the failure mode of the solder joints. When the Au layer was thin (0.1 µm), the dissolved Cu from the Cu/Ni UBM was able to inhibit the formation of AuSn4. When the Au layer was thick (0.65 µm), the dissolved Cu was not able to inhibit the formation of AuSn4. These AuSn4 enhanced the Ni consumption rate of the UBM. The presence of a large amount of AuSn4 inside the solder also weakened the solder because of the Au embrittlement effect. In view of these observations, the gold thickness on the Au/Ni surface finish must be kept to the minimum controlled in order to prolong the service life of flip-chip packages.

Key words: Flip chip, interfacial reaction, Au, solder

INTRODUCTION

Flip-chip soldering technology is the technology of choice for packaging high-performance chips. In this technology, solder joints are used to connect the chip and the substrate. On the chip side, the areas of the chip surface in direct contact with the solder have to be coated with the so-called under-bump metallurgy (UBM). On the substrate side, the areas of the substrate surface to be in direct contact with the solder have to be coated with a surface finish. Many different types of UBM and surface finish have been developed. These UBMs and surface finishes all have a wetting layer to enhance wetting with the solder and a diffusion barrier layer to avoid excessive reaction with the solder. For the surface finish, a layer of oxidation protection, typically Au, is deposited over the wetting layer to ensure that the substrates have an appropriate shelf life before assembly.

During soldering and the normal service life of a flip-chip device, the solder reacts with the UBM and surface finish. The interfacial reactions between solders and UBM as well as between solders and surface finishes had been studied quite intensively in the past.1–19 These studies, however, did not pay special attention to the influence of the reaction at one interface, such as the UBM/solder interface, on the reaction at another interface, such as the solder/surface finish interface. Recently, it had been pointed out that the reaction at one interface influenced the reaction at another interface.2 As the device size shrinks, the solder joints connecting the chip and the substrate become smaller. Hence, the distance between chip and substrate also becomes shorter. This decrease in the distance between the two interfaces will make the interactions between these two interfaces even more important. The first objective of this study is to look into this interaction across the two interfaces in flip-chip solder joints.

As mentioned earlier, the Au layer is often used as an oxidation protection layer in a surface finish. It is well known in electronic assembly technology that high Au content in a solder joint would weaken the joint.7,12,14 The amount of solder in a joint is proportional to r3 (r is the joint diameter), and the amount of Au in a solder joint is proportional to r2 if Au layer thickness is kept constant. It follows that the Au concentration in a solder joint is proportional to r−1.
Consequently, as the dimensions of the flip-chip solder joints shrink, the Au content in the solder joints will increase. In other words, for smaller solder joints, a thinner layer of Au might have to be used in order to keep the Au concentration in a safe level. The second objective of the study is to investigate the effect of Au thickness of the surface finish on the flip-chip solder joints.

**EXPERIMENTAL**

In this study, the UBM on the chip had a Cu/Ni/Al structure, as illustrated schematically in Fig. 1. The Cu and the Ni layers were sputter-deposited and were 0.8 µm and 0.5 µm, respectively. The surface finish on the substrate had the Au/Ni structure. Two different sets of surface finish thicknesses were used. The first set, denoted as THK for thick Au, had 0.65-µm Au and 5-µm Ni, and the second set, denoted as THN for thin Au, had 0.1-µm Au and 6-µm Ni. The solder was the 63Sn37Pb eutectic solder. The solder joints had a nominal diameter of 125 µm.

The chips and the substrates were assembled by reflowing in a reflow oven following a reflow profile commonly used by the industry. The peak reflow temperature was 213°C, and the period of time above melting point was 64 sec. The reflow condition for the first reflow (forming the solder balls on the chip) was the same as the reflow condition for assembling the chip and the substrate. The assembled samples were then kept in a high-temperature oven at 150°C for up to 2,000 h for a high-temperature storage test (HTST). After the HTST, the samples were mounted in epoxy and metallurgically polished in preparation for characterization. The interfaces for each sample were examined using scanning electron microscopy (SEM). The compositions of each phase were determined using electron microprobe analysis (EPMA) operated at 20 keV. In microprobe analysis, the concentration of each element was measured independently, and the total weight percentage of all elements was within 100% ± 1% in each case. The average value from at least three measurements was then reported.

Some of the HTST samples were pulled to fracture along the tensile direction using a universal tensile tester in order to identify the failure mode. The failure surface was examined by SEM.

**RESULTS**

**Microstructure after the First Reflow**

Before the chips were assembled with the substrates, the chips along with the deposited solder had gone through the first reflow to form solder balls on the chips. Figure 2 shows the UBM/solder interface after this reflow. The Cu layer in UBM had not been completely consumed, and scallop-type Cu6Sn5 formed over the remaining Cu layer. In addition, there were voids in the Cu layer. It is believed that these voids are Kirkendall voids formed because of the reaction of Cu and the solder. The formation of Kirkendall voids was due to the different diffusion rate between the Cu of the UBM and the Sn of the solder. Similar Kirkendall voids had been reported in the reaction between solder and bulk Cu.20

**Microstructure after Assembly**

Figure 3 shows the microstructures of the solder joint right after the chips were assembled with the substrate. For both the THN and THK surface finishes, Cu6Sn5 formed at the UBM/solder interface, and (Cu1–xNix)6Sn5 formed at the solder/surface finish interface. The Cu layer on the UBM had been completely consumed, and Cu6Sn5 at this interface was in direct contact with the Ni layer of the UBM. It is very interesting that (Cu1–xNix)6Sn5, instead of Ni3Sn4, formed at the solder/surface finish interface.