Growth and Characterization of GaN Thin Films on SiC SOI Substrates

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SiC semiconductor-on-insulator (SOI) structures have been investigated as substrates for the growth of GaN films. The SiC SOI was obtained through the conversion of Si SOI wafers by reaction with propane and H₂. (111) SiC SOI have been produced by this carbonization process at temperatures ranging from 1200 to 1300°C. X-ray diffraction (XRD) and infrared spectroscopy (FTIR) are used to chart the conversion of the Si layer to SiC. Under our conditions, growth time of 3 min at 1250°C is sufficient to completely convert a 1000 Å layer. XRD of the SiC SOI reveals a single SiC peak at 2θ = 35.7° corresponding to the (111) reflection, with a corrected full width at half-maximum (FWHM) of ~590±90 arc-sec. Infrared spectroscopy of SiC SOI structures obtained under optimum carbonization conditions exhibited a sharp absorption peak produced by the Si-C bond at 795 cm⁻¹, with FWHM of ~20–25 cm⁻¹. Metalorganic CVD growth of GaN on the (111) SiC SOI was carried out with trimethylgallium and NH₃. The growth of a thin (~200 Å), low temperature (500°C) GaN buffer layer was followed by the growth of a thick (~2 μm) layer at 1050°C. Optimum surface morphology was obtained for zero buffer layer. XRD indicates highly oriented hexagonal GaN, with FWHM of the (0002) peak of ~360±90 arc-sec. Under high power excitation, the 300°C photoluminescence (PL) spectrum of GaN films exhibits a strong near band-edge peak (at λp ~371 nm, with FWHM = 100–150 meV) and very weak yellow emission. Under low power excitation, the 370 nm PL emission from the GaN/SiC SOI structure increases rapidly with SiC carbonization temperature, while the yellow band (~550–620 nm) correspondingly decreases.

Key words: Carbonization, characterization, GaN, photoluminescence, SiC, SOI

INTRODUCTION

The rapid development of III-V nitride technology is leading to major advances in related devices, including commercial blue and multi-color light-emitting diodes (LED). Recently, the feasibility of blue semiconductor diode lasers has been reported. Due to the absence of commercial GaN bulk crystals, the investigation of alternate substrate materials is a very important task. The main requirements for an appropriate substrate for GaN epitaxial growth are:

- Dimensional lattice-matching;
- Thermal expansion coefficient matching; and
- Availability in large quantities, with large diameter and at low cost.

The substrate of choice to date has been sapphire (α-Al₂O₃) because of its commercial availability and excellent surface preparation. However, sapphire has a very large lattice mismatch with wurtzite GaN: ~33° for the aligned basal planes and >20% considering a 30° rotation of the GaN basal plane with respect to the sapphire basal plane. This inevitably leads to a large defect density of GaN epitaxial layers. Hexagonal (6H)-SiC offers a much smaller lattice mismatch (3.5%), which, although too large for perfect heteroepitaxy, is small enough to reduce the dislocation density significantly. 6H-SiC, however, suffers from limited availability, small diameter (<5 cm) substrates, and very high cost. In this paper, we discuss an alternative substrate approach for epitaxial growth of GaN, which has the potential of providing large area, low cost 3C-SiC (111) substrates with fairly small lattice mismatch (3.5%). An additional consideration in heteroepitaxy is the mismatch
in linear thermal expansion coefficient between growth layer and substrate over the growth temperature range. The average expansion coefficient \(4.9 \times 10^{-6}/K\) for GaN is quite well with the value of \(4.7 \times 10^{-6}/K\) for 3C-SiC. On the other hand, the only expansion coefficient value over the same temperature range related to sapphire which we have found in the literature is that of alumina, which is \(9.25 \times 10^{-6}/K\). This value probably understates the expansion mismatch, as the expansion coefficient of alumina also changes much more with temperature than that of GaN. The combination of these two considerations clearly indicates that strain in the GaN overlayer should be significantly reduced by the use of a 3C-SiC substrate.

We have fabricated SiC SOI structures and utilized them as substrates for GaN growth. As shown in Fig. 1, the starting point for SiC SOI is a silicon SOI wafer consisting of a normal Si substrate, an oxide layer and a thin Si device layer. The Si SOI structure is produced either by thermal bonding and etch back of two Si wafers or by oxygen ion implantation. The thin Si device layer (from several hundred to a few thousand Å) can be rapidly and completely converted to cubic (3C) SiC by a chemical vapor deposition (CVD) process through exposure to propane or other carbon-containing gases at high temperature. This minimizes the formation of voids and other defects which accompany the carbonization of conventional Si substrates, where Si atoms can diffuse out from the bulk along \(<111>\) planes until the surface is completely sealed. Next, a thick GaN layer of several μm can be grown by a variety of deposition techniques. The SOI substrate has several additional advantages over the use of conventional Si substrates. The presence of the oxide layer is beneficial in absorbing growth-generated stress and dislocations. The oxide layer can also provide improved performance through electrical isolation between devices, as in Si SOI devices and circuits. Finally, if the GaN film is grown thick enough (>100 μm) to be self-supporting, the oxide can serve as a “quick-release” layer through selective etching.

Si SOI device technology is currently experiencing intense development for commercial low power and very large scale integration (VLSI) applications, resulting in the rapid development of SOI substrates in terms of wafer diameter, quality, and cost. Therefore, the approach of using the SiC SOI structure as a substrate for GaN growth can directly benefit from the progress obtained by the much larger SOI community.

**SiC SOI FORMATION AND CHARACTERIZATION**

The use of insulating substrates for the CVD growth of cubic SiC has been reported by Pazik et al. and Tang et al., utilizing Si-on-sapphire (SOS) and by Steckl et al., utilizing the SOI structure discussed above. A similar SiC SOI has been pursued by Yang et al., where the use of MBE growth for the carbonization was investigated. In the work reported here, we have utilized (111) Si SOI structures with a thin Si (111) device layer (900–1000 Å), a 1 μm SiO₂ layer and a Si (100) substrate. The crystal orientation of the Si (111) layer was tilted 2.4° off-axis. The starting SOI was produced by thermal bonding and etch back. To provide the 0.1 μm Si device layer with high uniformity over the wafer area required a specialized plasma etching process. SiC growth on the (111) Si was selected on the basis of superior results with growth of thicker 3C-SiC films directly on (111) and (100) Si substrates. In addition, the (111) SiC surface, which closely resembles the c-plane of 6H-SiC, is a better match for subsequent growth of III-N films.

The Si-to-SiC conversion was performed in a rapid thermal chemical vapor deposition (RTCVD) reactor which restricted exposure to high temperature to only the few minutes needed for in-situ cleaning and complete carbonization. Additional information on the operation of the RTCVD reactor for SiC growth can be found elsewhere. Figure 2 contains a typical process diagram. After wet chemical cleaning, the samples