INTRODUCTION

Bonding III-V semiconductor thin films with Si substrates using the epitaxially lifted-off (ELO) technique has been a subject of great interest in recent years. Because the lifted-off films are usually very thin, the III-V devices can be more easily integrated with Si devices using this technique than using other wafer bonding methods. To date, a number of devices such as solar cells, light emitting diodes (LEDs), laser diodes, heterojunction bipolar transistors (HBTs), metal semiconductor field-effect transistors (MESFETs), and high electron mobility transistors (HEMTs) have been fabricated on Si substrates using this technique. However, the ELO technique relies on Van der Waals bonding between the film and the substrate. It often suffers from poor mechanical and electrical properties. To improve bonding, Yablonovitch et al. and Fathollahnejad et al. used Pd or Pd/Ge coated Si substrates and good bonding was formed between the GaAs thin film and the substrate after annealing. The metal layer also provided good ohmic contact to the GaAs layer. For all approaches mentioned above, however, the vertical conduction between the III-V semiconductor film and the Si substrate was poor. A good conduction between the two would greatly simplify the wiring requirement and the integration process. So, in this study, we set out to investigate a metal structure that can be used in the ELO process to provide ohmic contact to both the lifted-off GaAs thin film and the Si substrate.

It has been reported that Pd/Ge can penetrate the surface native oxide of GaAs during annealing and provides low-stress ohmic contact to GaAs. On the other hand, palladium silicide makes a good ohmic contact to Si. The silicide contact is shallow and smooth and does not cause spiking behavior which is commonly seen with aluminum contacts. So, a Pd/Ge/Pd metallic structure is used in this study. The electrical behavior of the interface between the GaAs film and the Si substrate was examined by the current-voltage (I-V) measurement at various temperatures. Secondary ion mass spectrometry (SIMS) and x-ray diffraction analyses were used to study the interface compound and the formation of the metal-lurgical bonding. Finally, we fabricated an ELO stripe geometry diode laser on n-Si substrate with the back-side contact on Si substrate. Good laser performance with comparable characteristics as conventional laser diodes on GaAs substrates was obtained.

Key words: Epitaxial lift-off (ELO) method, laser diode, n-type GaAs

EXPERIMENTS

The GaAs film, which was to be lifted off, was grown by molecular beam epitaxy (MBE). The layer was 1 µm thick with a Si doping of $2 \times 10^{18}$ cm$^{-3}$ and was grown on top of a 100Å thick AlAs sacrificial layer. Rectangular $500 \times 350$ µm$^2$ mesa structures with a
Low-Resistance Vertical Conduction Across ELO n-GaAs Film and Pd/Ge/Pd Coated Si Substrate

6000Å etched depth were formed. Au-Ge contact with dimensions of \(120 \times 120 \, \mu m^2\) was then defined on the mesa top. The samples were annealed by rapid thermal annealing (RTA) at 400°C for 10 s. The samples were then covered with Apiezon W black wax, which was used to protect the samples surface and provide mechanical support in later processes. A (100) n+Si substrate with a resistivity of 0.01-1 Ω-cm was used as the host substrate in the ELO process. Multilayer metal structures of Pd(1000Å)/Ge(1250Å) and Pd(1000Å)/Ge(1250Å)/Pd(2500Å) were deposited on separate Si substrates by an electron-gun deposition system under a base pressure <8 × 10^{-7} Torr. The metal coated Si substrates were dipped in dilute HCl solution before being attached with the ELO film. The GaAs film was lifted from the substrate by soaking in dilute HF solution. Before the bonding process, the processed n-GaAs film with black wax was dipped in HCl and HF. Then the GaAs film and the Si substrate were bonded together by Van der Waals bonding. A proper pressure was applied on these samples to squeeze out the deionized (DI) water at the interface. After the bonding process, the black wax was removed and then a 4000Å Al layer was evaporated on the back of the Si substrate for ohmic contact. The samples were then annealed at 400°C for 30 min under a forming gas ambient. This annealing procedure caused the formation of metallurgical bonding between the grafted film and the Si substrate and at the same time sintering of the backside Al contact. These samples were diced into ~5 × 5 mm² for electrical measurement.

### RESULTS AND DISCUSSION

#### Electrical Characterization

For I-V measurement, three different samples were used. Sample A was the reference sample with the GaAs film on GaAs substrate without being lifted off. For samples B and C, Pd/Ge and Pd/Ge/Pd were used as the bonding agents, respectively, in the bonding process. Figure 1 shows the I-V curves measured at room temperature for samples A, B, and C. While samples A and C show good vertical conduction, sample B is non-ohmic. The series resistance of the three samples are shown in Table I. The resistance for the sample with Pd/Ge/Pd interlayer is comparable to that of the reference sample. So an additional layer of Pd between Pd/Ge and Si causes the formation of ohmic contact to Si. Since the bonding and the contact formation are caused by the Pd/Ge/Pd metal layer, the I-V characteristics are independent of crystal orientation. No precise alignment between the ELO film and the host substrate is needed. Figure 2 shows the temperature dependence of the vertical conduction behavior. Good ohmic behavior is maintained even for temperatures as low as 50K.

#### Material Structural Characterization

The interface reaction between the Pd/Ge/Pd layer and...