H.263 VIDEO CODEC IMPLEMENTATION BASED ON MULTIMEDIA DSP

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Abstract This letter introduces the implementation of H.263 video codec based on multimedia DSP TM1300, and discusses several key problems related to video coding.

Key words Video communication; H.263; Algorithm optimization; TM1300

I. Introduction

ITU-T published the H.263 recommendations in 1996 in order to promote the multimedia communication services on narrow-band channel. H.263+\([1]\) and H.263++ were further issued in 1998 and 2000, respectively, and offered nearly 20 more options for improvement.

This letter introduces the methods of implementation of H.263 codec based on DSP (Digital Signal Processor), the constructions and algorithm optimization of video coding, multi-thread setting, and communication interface to the modem.

II. The H.263 Codec Threads

The signal stream diagram of the H.263 codec based on DSP is illustrated in Fig.1. It is a set of programs used for video coding in C language.

As shown in the figure, first, the analog video signal coming from a camera is digitized by A/D converter at YUV 4:2:0 digital video format—QCIF, and restored into the input buffer in TM1300\([2]\). Secondly, the H.263 coder reads out the data in the input buffer and encodes them. The compressed data are then passed on into the send buffer. Finally, serial interface unit reads out the data from the send buffer and sends them into the send-unit for modem. At the same time, decoder receives the data from PSTN channel, decodes and displays it on the screen of a monitor.

![Fig.1 Video codec program stream based on DSP](image)

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As a video coding software on DSP, it utilizes the multitasking capacities provided by the pSOS system. And the main program framework is constructed in the multi-threading manner\textsuperscript{[3]} in order to fulfill the requirement for real-time video communication. The threads distribution is also showed in Fig.1.

**III. H.263 Codec Based on TM1300**

1. The architecture and capacities of TM1300

The TM1300 is a high performance multimedia DSP chip made by Philips, which can process audio, video, data and other control signal simultaneously.

A highly efficient VLIW(Very Long Instruction Word)core processor—DSPCPU in TM1300 is used to realize concrete algorithm and to control other units on the chip. When the CPU runs under the embedded real-time operating system—pSOS, it can provide interruption and communication between on-chip units. The DSPCPU makes use of the VLIW instruction system, with a system clock frequency higher than 180MHz. Five operations can be finished within one machine clock cycle, and each operation includes several PdSC(Reduced Instruction Set Computer) operations. In addition, TM1300 also includes some important units, such as a high performance inner bus, an easily accessible inner memory system, 16kB data caches and 32kB instruction caches.

TM1300 has an I\textsuperscript{2}C bus, a PCI bus as well as SSI interfaces for connecting with devices out of the chip. I\textsuperscript{2}C bus interface can be used to ensure that TM1300 works independently without the PC support. The highest running frequency of PCI interface is 33MHz, and it benefits from connection with a computer. Synchronous Serial Interface(SSI) is another communication interface, providing the bi-directional channel between PSTN (or ISDN) and the TM1300 system.

For convenient multimedia applications, TM1300 also has an audio I/O and a video I/O interface. The video input unit can directly receive and send ITU-R656/601 format digital video data.

2. The optimization of coding algorithm

In order to ensure real-time processing of video signals, the main coding and decoding algorithms must be optimized at different levels.

(1) **Three optimization levels** Optimization of video coding program can be divided into three levels, from up to down: overall program framework, concrete algorithm and instruction optimization. Moreover, the independence between levels benefits the design of each level, re-developing and transplanting, as long as we keep the interface between levels unchanged.

The procedure of instruction optimization includes two methods: automatic optimization by compiler and manual optimization by programmer. The compiler of TM1300 can optimize user programs according to its RISC structure, and programmer’s manual optimization can help to overcome the compiler’s limitations.

(2) **Normal methods for TM1300 optimization** TM1300 will improve the program efficiency with its developmental tools. At the first step, we can use the compiler for automatic optimization. For instance, one may use grafting based lateral information, and global optimization technique to get better coding performance. Global optimization can be initiated by some compiling parameters in the TM1300 SDE (Soft Development Environment) or integrated environment—code warrior. At the second step, we can remove “if” sentences, release recycle sentences and so on.