DESIGN AND RESEARCH OF QUASI-PLANAR SELF-ALIGNED SILICON AVALANCHE ELECTRON EMISSION ARRAY*

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Abstract The device structure and technical processings of quasi-planar self-aligned silicon avalanche electron emission array are introduced. The processing step at the edge of electron emission region is about 10nm only and the width of self-aligned current channel of shallow As implantation is about 3μm. Its I-V characteristics show a larger linear region and lower series resistance than that of the previous silicon avalanche electron emission devices. Some of the electron emission characteristics are also discussed in this paper.

Key words Vacuum microelectronics; Electron emission; Cold cathode

I. Introduction

Recently the research of vacuum microelectronics becomes a rising area in microelectronics. The external field electron emission array device with micro-tip structure has been achieved important progresses. However, its fabrication processes are quite difficult. At the same time problems in uniformity and repetition still exist. Especially they will be easily damaged in the later processes[1]. Therefore the research of planar internal field electron emission array devices are also carrying out. The research of planar internal field electron emission array devices within new structure and new kinds of material will promote the development of cold electron emission device with high performance.

Silicon avalanche cathode (SAC) is a planar internal field electron emission device based on IC planar technology. There exist some processing steps from a few decades to a few hundreds of nanometer in depth because of several times of oxidation, diffusion and photolithography in processing. The depth of processing step near the rim of electron emission area of shallow p-n junction is about the same order with junction depth. Recent years Lu, et al. reported the relationship of current distribution and electron emission characteristics with device surface topology of SAC using two dimensional device simulation PISCES-IIB[2,3]. The results show that the processing steps cause the non planar surface topology of the device. It will cause the current crowding effect near the rim of the shallow p-n junction and increase the on resistance when the applied reverse voltage is increased. It will also cause current punch-through effect which will reduce the effective reverse bias current and reduce the emission efficiency.

In this paper the device structure and processing steps of quasi-planar self-aligned silicon avalanche electron emission array is introduced. It has a quasi-planar electron emission area

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with a depth of processing step about 10nm. The positive electrode region of electron emission diode (p+ region) and its negative electrode region (n+ contact region) are formed by self-aligned technology. The shallow As implantation layer between these two regions forms shallow p-n junction and self-aligned n+ current channel with good uniformity and 2-3 µm in width.

The experimental results show that it has a larger linear region in I-V characteristics than that of SACs in previous structures and a better uniformity in electron emission.

II. Device Structure and Fabrication Processing

The device structure of a cell of quasi-planar self-aligned SAC is shown in Fig. 1. The starting material is p-/p+ silicon epitaxy wafer in (111) direction. The resistivity and thickness of p- epilayer is 0.8 to 2.0 Ω·cm and 7-10 µm respectively and the resistivity of p+ silicon substrate is lower than 0.01 Ω·cm.

The main processing steps of quasi-planar self-aligned SAC are shown in Fig. 2. First a layer of oxide with thickness of 500nm is thermally grown on p-/p+ substrate, then a layer of Si3N4 with thickness of 120nm is deposited on this oxide layer by LPCVD technology. A selected etching of Si3N4 is carried out to keep the Si3N4 just on the position of n+ current channel region (6µm in width) forming the self-aligned mask. Then the n+ contact region oxide window is opened by photolithography and phosphorous pre-deposition diffusion is carried out. Then a short time (15min) phosphorous drive-in is carried out in dry oxygen at 1150°C. The p+ diode region diffusion window is also opened by photolithography but it is self-aligned by Si3N4 layer. Boron ion-implantation is carried out with a dosage of 2 x 10^{24} cm^{-2} at 60 keV. After removing all the remaining oxide and Si3N4 layer, n+ contact region and p+ diode region is under drive-in diffusion and reoxidation simultaneously at 1150°C 70min forming a 500nm oxide. An As ion-implantation window is opened across the p+ region and part of n+ contact region. A low energy (< 25keV) As ion-implantation with a dosage of 2 x 10^{14} cm^{-2} is carried out and then annealed in N2 gas at 800°C 2 h. In order to reduce the average range of As implantation a thin oxide layer (10~15 nm) is used as a shield layer. The depth of the shallow junction formed by As implantation layer and p+ region is about 30nm. Its avalanche breakdown voltage is always between 6-10V and can be changed by changing the doping density of the p+ region.

Because Si3N4 self-aligned technology is used and p+ diode positive region, n+ contact region and current channel region are reoxidized at the same processing steps, a new structure SAC with low processing steps between different regions and with a short self-aligned current channel is realized.

III. Analysis of Device Surface Topology and Some Experimental Results

Because the doping densities of n+ contact region, p+ region and current channel region are different, the oxidation rate at reoxidation processing step is different\(^\text{[4]}\). According to the variation of oxidation rate influenced by processing conditions and doping densities, the thickness of the oxide and the heights of the surface steps in different regions can be calculated by the oxide growth model. The calculating values of the heights of processing