Analog Design Issues in Digital VLSI Circuits and Systems

GUEST EDITORIAL

Introduction

All electronic signals are fundamentally analog in nature, where these analog signals are constrained to specific voltage levels in digital circuits. The application of a binary constraint has accelerated the development of sophisticated digital VLSI systems. However, the requirement for high speed and, more recently, ultra-low power in digital integrated circuits and systems has necessitated a new design strategy, that of applying analog design techniques to digital systems in order to extract the greatest levels of performance. This analog methodology must be applied to digital circuits while maintaining the complexity requirements inherent in VLSI/ULSI-based systems. This special issue is focused on the topic of applying analog design methodologies to VLSI complexity digital circuits so as to maximize system performance. We hope to “pull the curtain back” on modern digital integrated circuit design by addressing some challenging issues associated with the not so binary aspects of the art of designing digital VLSI circuits. No longer should the design of digital integrated circuits be considered as simple as creating a net list, or as automated as a Boolean simplification.

Further elevating the need for considering the analog behavior of digital systems are the following trends. The feature size of VLSI circuits continues to decrease at a rate of thirty percent per year as it has for the past fifteen years. Operational speeds have increased by about one order of magnitude every eight years. Further, since the mainstream computing paradigm has not changed significantly since the mid 1960’s, much of the burden for the increase in calculation speed has been placed on the speed of the logic circuits. The calculation speed of today’s microprocessor can exceed 500 MIPS. The capacity of current memory circuits approaches the one gigabit complexity mark. The power supply voltage has been reduced to below 1.5 volts. These trends, fueled by the competitive consumer markets, demand innovation from the community of integrated circuit designers, and are expected to continue as long as microelectronics technologies and computing paradigms can respond with suitable innovative solutions.

The technical problems that arise from this speed-density treadmill are formidable, let alone the logistics problems associated with managing the development of these high complexity systems. Due to the complexity of these systems-on-a-chip, the pressures for accuracy and consistency in timing analysis and clock distribution have never been higher. Most high performance CPU’s employ phase locked loops in order to generate high fidelity clocks which must coexist with noisy digital circuits. Circuit designers need additional degrees of freedom in distributing and analyzing the clock signals. The deceptively simple choices of circuit thresholds and wave shapes fall far short of accuracy requirements. The push for portability and performance in the consumer market requires the development of novel high speed, low power circuit concepts which exploit a particular process technology. As a consequence, chip designers are hungry for analysis techniques for estimating the speed and power dissipation characteristics of a system. The field of asynchronous state machine design requires new arbiter design techniques. The pressure on time to market has sparked interest in characterization and simulation of worst case manufacturing conditions early in the design cycle to assure first pass success.

Clearly, as evidenced by the contributions to this special issue, the industrial and academic communities involved in integrated circuit design have responded to these complexities in supporting the market place. The eleven contributions to this special issue touch three major areas of integrated circuits including simulation and analysis, novel design techniques, and robust design. Two papers describe research being developed in American industry while nine papers present research from universities around the world. These papers originate from diverse regions of the world including, in alphabetical order, France, Germany, Spain, Turkey, and the United States. Through this special issue the editors portray a cross section of research which exploits the analog characteristics of digital integrated circuits.
Circuit Analysis and Simulation

Perhaps one of the most significant advantages that digital circuit designers have as compared to their peers in analog design is the wealth and maturity of simulation and analysis tools for predicting and verifying the performance of their digital circuits. The area of simulation and circuit analysis is addressed here by four papers, each of which enhance the capabilities of computer-aided design and analysis.

V. Chandramouli and Karem A. Sakallah discuss the proper choice of threshold voltages to avoid the occurrence of negative delay in simulation. Negative delay often occurs in timing analysis as a result of the assumed signal thresholds and wave shapes. The authors impose six basic constraints on the delay and transition time thresholds in their analysis, and ultimately conclude that unity differential gain points are the most desirable thresholds for timing analysis. The methodology described in this paper can be used to improve the accuracy of timing simulations, enabling the designer to squeeze every ounce from a target clock cycle. Moreover, the results are general enough to be applied to any logic family or RLC delay line.

Victor Adler and Eby G. Friedman develop expressions for calculating the delay and power dissipation for CMOS inverters driving resistance-capacitance loads. In contrast to the method proposed by Chandramouli and Sakallah, the standard 50%, 10%, and 90% switch points for delay and transition time are used. Comparisons to SPICE are presented. The authors present simple yet effective expressions which consider the effects of highly resistive lines on active devices while being easily integrated into a computer-aided simulation environment. These expressions expand the capacity of a design team to analyze the timing and power relationships in large integrated circuits.

U. Bretthauer and E.-H. Horneber present their BRASIL simulator which enables accurate and fast timing analysis through partitioning and numerical iteration. The simulator partitions the task into switch level models for steady state logic calculation, fast macro-models for logic delay, capacitance and time-variant conductance networks for more detailed circuit timing analysis of custom design styles, and finally circuit simulation for the most detailed mixed signal analysis. The program, under the supervision of the user, manages the coupling of the partitions to integrate a coherent, fast, and accurate timing analysis of complex digital circuits.

Eby G. Friedman and J. H. Mulligan, Jr. arrive at closed form expressions describing the delay characteristics of RC tree networks. The authors extend the Penfield, Rubenstein, and Horowitz algorithm to handle ramp inputs. This work is particularly significant since the shape of the signal is incorporated into the delay analysis. The delay expressions and their associated upper and lower bounds are presented.

Novel Circuit Design Techniques

The second major area discussed in this special issue includes novel circuit design. These research results are clear responses to the competitive market demands of speed, portability, and time-to-market. In this section we get a sampling of certain innovative design techniques that are presently under investigation.

Ismail Enis Ungan and Murat Askar propose a CMOS design technique for low voltage, high speed VLSI circuits. The technique allows circuit speeds to exceed standard static CMOS while offering lower switching noise, thereby minimizing the problem of integrating high fidelity analog functions onto high speed digital chips. Due to the importance of minimizing static power dissipation, current-mode logic has become a viable alternative to standard CMOS design in many high speed applications.

Micah C. Knapp, Peter J. Kindlmann, and Marios C. Papaefthymiou examine the implementation and evaluation of adiabatic logic that enable energy savings over standard CMOS. A review of adiabatic logic styles known to those experienced in the art is given. The authors use 2N2P circuit structures as a vehicle to address design problems at the logic and systems levels. The energy consumption of the arithmetic units implemented with 2N2P and CMOS circuits is compared. This paper sheds light on a design style which has yet to find mainstream acceptance, but shows significant potential in enabling ultra-low power, portable electronics of the future. In contrast to the current mode CMOS logic proposed by Ungan and Askar which excel in high speed applications, these circuits address the energy conservation problem at the expense of speed.

Haydar Kutuk and Sung-Mo Kang present a novel example of the merging of analog and digital design. They merge the design of analog filters into a digital design methodology. The area of field programmable design continues to be dominated by digital circuits, but Kutuk and Kang offer a field programmable array which enables fast designs of switched capacitor