A Current Conveyor based Field Programmable Analog Array

CHRISTOPHE PREMONT
CIMIRLY INSA Lyon, Bat 401, 3eme etage, 20 Av. Albert Einstein, 69621 Villeurbanne Cedex, France
premont@cegely.insa-lyon.fr

RICHARD GRISEL
CPE, LISA EP-CNRS 0092, 43 Bd du 11 novembre 1918, BP 2077, 69616 Villeurbanne Cedex, France
grisel@cpe.fr

NACER ABOUCHI
CPE, LISA EP-CNRS 0092, 43 Bd du 11 novembre 1918, BP 2077, 69616 Villeurbanne Cedex, France
abouchi@cpe.fr

JEAN-PIERRE CHANTE
CEGELY INSA Lyon, Bat 401, 3eme etage, 20 Av. Albert Einstein, 69621 Villeurbanne Cedex, France
chante@cegely.insa-lyon.fr

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Abstract. An approach for designing a Field Programmable Analog Array (FPAA) is described. The analog array is based on current conveyors and benefits from two major interests: a large bandwidth and a low number of discrete components needed for the implementation of analog functions. An Analog Elementary Cell (AEC), based on current conveyors has been developed, and it is associated with programmable resistors and capacitors. Analog functions can be performed programming several AECs as current-mode amplifiers, analog multipliers, etc. The main purpose of this paper is to introduce current conveyor based analog blocks which are very-well suited for the implementation of FPAA. A particular interconnection architecture is addressed using current conveyors as switches. The major key feature of the proposed approach is that current conveyors are used as active elements and switching elements. A new topology based on the developed AEC is proposed and should be shortly validated.

Key Words: Field Programmable Analog Array, current conveyor

1. Introduction

A FPAA consists of a number of reconfigurable analog elementary cells which can be interconnected by a programmable architecture. If one considers the great improvement that FPGAs (Field Programmable Gate Arrays) represents for digital design, one can imagine that an analog counterpart for this type of circuit would provide electronic designers with a very efficient and powerful tool. However, FPAA have not been developed as much as FPGAs because of a lack of real market and because a number of limitations such as precision, offsets, noise, etc.

The key feature of FPAA are flexibility and programmability. This paper deals with the implementation of basic analog functions, investigating new programmability features and topology. Based on current conveyors, this approach provides designers with programmable elementary cells. This paper focuses more on the elementary cell of the analog array than on the analog array itself because the work is still in progress.

Firstly, Section 2 introduces the current conveyors and their applications. Section 3 describes the analog elementary cell (AEC) and the programmable elements. Then, Section 4 focuses on AEC based application in order to show the real potentialities of the proposed approach. The analog array topology and programmable features are addressed in Section 4.
2. Current Conveyor

A current conveyor (CC) \([1–3]\) is a three terminal device which performs many useful analog signal processing functions (see Table 1) when arranged with other electronic elements in specific circuit configurations. The operation of this device is such that if a voltage is applied to input terminal \(Y\), an equal potential will appear on the input terminal \(X\). In a similar fashion, an input current forced into terminal \(X\) will result in an equal current flowing into terminal \(Z\). Fig. 1 shows the schematic circuit of the second generation current conveyor (CCII), DC biased by two currents \(I_0\).

By using the equivalent schematic presented in Fig. 2, which gives the input and output impedance, the behavior of the CC can be described by a voltage transfer and a current transfer as follows:

\[
V_X = \alpha V_Y \tag{1}
\]

\[
I_Z = \pm \beta I_X \tag{2}
\]

\((\alpha, \beta \approx 1)\)

For this paper, only the second generation positive current conveyor (CCII+) is considered \((\beta = 1)\). It could be demonstrated that \(\alpha\) and \(\beta\) depend on the equivalent load at respectively \(Y\), \(X\) and \(Z\) terminal. (R1 and C1, R2 and C2, R3 and C3 in the Fig. 2).

\[
\alpha = \frac{R_2}{R_2 + R_X} \tag{3}
\]

\(\text{Table 1. Current conveyor applications.}\)

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<tr>
<th>V-Controlled V-Source</th>
<th>Current-Amplifier</th>
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<tr>
<td><img src="image1" alt="V-Controlled V-Source" /></td>
<td><img src="image2" alt="Current-Amplifier" /></td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>V-Controlled I-source</th>
<th>Current-Differentiator</th>
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<tr>
<td><img src="image3" alt="V-Controlled I-source" /></td>
<td><img src="image4" alt="Current-Differentiator" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I-Controlled I-source</th>
<th>Current Integrator</th>
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<tr>
<td><img src="image5" alt="I-Controlled I-source" /></td>
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</tbody>
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<tr>
<th>I-Controlled V-source</th>
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<tbody>
<tr>
<td><img src="image7" alt="I-Controlled V-source" /></td>
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</tbody>
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