Complete Clock-Feedthrough Cancellation in Switched-Current Circuits by Combining the Replica Technique and the N-step Principle

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Received November 14, 1995; Accepted July 8, 1996.

Abstract. This paper begins with an analysis of the charge injection error in the second-generation current memory cell. By combining the circuit replication technique and the n-step principle, a new scheme for simultaneously cancelling both signal-dependent and signal-independent charge injection errors in second-generation switched-current circuits is proposed. SPICE simulations are used to verify the feasibility and effectiveness of the proposed cell for tackling the charge injection problem. Major merits of the proposed cell include capability to meet high precision requirements and applicability to any second-generation switched-current circuit configuration.

Key Words: Switched-current circuits, clock-feedthrough cancellation, second-generation SI circuits.

1. Introduction

The newly developed switched current (SI) technique [1] for analogue sampled-data signal processing has attracted considerable attention in recent years. The SI technique has such advantages as compatibility with standard digital processes and capability of operating in current domain with low supply voltage that make it a promising alternative to the conventional switched-capacitor technique in the monolithic implementation of mixed analogue and digital VLSI. However, the charge injection (also known as clock feedthrough (CFT)) problem [2] has proven to be very serious in switched-current systems.

It has been known that the charge injection error in SI circuits consists of two parts: signal independent part and signal dependent part. The former one is just a pure offset but is large in magnitude among the total error, while the latter one is small in magnitude but varies with different signal levels. To solve the charge injection problem, a number of charge injection cancellation approaches have been proposed, notably the circuit-replication technique [3] which was proposed by Yang et al. to eliminate the signal-independent CFT error in the first-generation SI circuits. Most of the reported replica-based techniques are devoted to solving charge injection problems in the first-generation circuits, e.g., signal-dependent CFT cancellation [4] and total CFT compensation [5]. Recently a "dummy circuit" technique [6] which is based on the circuit-replication technique [3] has been proposed to eliminate the signal-independent CFT error in second-generation SI circuits. However, it still leaves the signal-dependent part of the error uncancelled, and as a result circuit accuracy seems not adequate enough for high precision applications. For cancelling the signal-dependent CFT error in second-generation SI circuits, an elegant and simple n-step scheme has been proposed recently [7]. Although this n-step scheme can suppress the signal dependent CFT error to a higher order, it is unable to clear the DC offset residue, unless it is applied to circuit configurations which employ pairs of memory cells, e.g., integrator loops, unit delay cells, differential circuits, etc. However, in the case of single-ended circuits, this DC offset will occur and cannot be cancelled automatically in odd order cascades of memory cells. This could arise in sample-and-hold cells, delay cells (series or parallel) or in data converters employing memory cells. Obviously the presence of DC offsets will seriously degrade circuit performance. Thus an effective total CFT error cancellation approach for general second-generation SI circuits is still on demand. Recently a total CFT compensation technique for second
generation circuits has been reported [9]. However, its circuit configuration is too complicated and its accuracy depends heavily on the match of transistors which is hard to achieve in practice.

In this paper, a new scheme is proposed which combines the replica technique and the n-step principle to cancel both the signal-independent (DC) offset and signal-dependent (AC) distortion errors in second-generation SI circuits. It should be noted that the proposed scheme can achieve high precision requirements and is suitable for any second-generation SI circuit configuration.

2. Charge Injection in Second Generation SI Circuits

2.1. Charge Injection Effects in Current Memory Cell

Figure 1 shows the basic second-generation current memory cell. The charge injection error is caused by the capacitive coupling of the clock signal $\phi_t$ through the parasitic gate-to-diffusion overlap capacitance of switch transistor $M_S$ and the injection of charge from the switch transistor channel to the gate of memory transistor $M$, when switch $M_S$ is turned off. The effect can be represented by an error voltage $-\delta V$ superposed on the gate of $M$, which directly causes an error current $\delta (I + i)$ on the output. As shown in reference [2], the total charge injected into the gate of $M$, which has the capacitance $C_g$, can be written as

$$\delta = \alpha \left( V_{H} - V_{gs} - V_T - \frac{2}{3} V_T^2 \right) C_{CH}$$

$$+ \frac{C_{OL}}{2} (V_H - V_L)$$

(1)

where $V_H$ and $V_L$ are the high excursion and the low excursion of switch gate voltage respectively, $C_{CH}$ and $C_{OL}$ are the switch channel capacitance and switch gate-diffusion overlap capacitance, $V_T$ is the threshold voltage with zero bias, $\alpha$ is the fraction of the total switch channel charge injected onto the gate of $M$, $V_T$ is the bulk threshold parameter, and $V_{gs}$ is the gate voltage of the memory transistor during the sampling phase assuming that memory transistor $M$ works in the saturation region.

$$V_{gs} = V_T + \sqrt{\frac{2(I + i)}{\beta}}$$

(2)

The error voltage $\delta V$ is given by

$$\delta V = \frac{q}{C_g}$$

(3)

Substituting Eqns. (1) and (2) into Eqn. (3), $\delta V$ can be expressed as

$$\delta V = K_a - K_b \sqrt{\frac{2(I + i)}{\beta}}$$

(4)

where

$$K_a = \frac{C_{CH}}{C_g} \left( V_H - \left(2 + \frac{2}{3} \right) V_T \right)$$

$$+ \frac{C_{OL}}{2C_g} (V_H - V_L)$$

and

$$K_b = \frac{C_{CH}}{C_g} \left( 1 + \frac{2}{3} \right)$$

It can be seen from Eqn. (4) that the error voltage is not a constant but is a function of the input current signal. Therefore the resulting output error current due to charge injection is

$$\delta (I + i) = (I + i) - \frac{\beta}{2} (V_{gs} - \delta V - V_T)$$

$$= \delta_{DC} + \delta_{AC}$$

(5)

where

$$\delta_{DC} = -\frac{\beta}{2} K_a^2 - (K_b^2 + 2K_a)I$$

$$+ K_b (1 + K_b) \sqrt{2} \beta I$$

(6)

$$\delta_{AC} = -(K_b^2 + 2K_a)i + K_b (1 + K_b) \sqrt{2} \beta I$$

$$- \left[ \frac{(i/I)^2}{2} - \frac{(i/I)^3}{8} + \frac{(i/I)^4}{16} - \cdots \right]$$

(7)

It can be seen that the total charge injection error in the second-generation current memory cell is composed of two parts. One part is the DC offset term (Eqn. (6)) which does not depend on the input current signal, but depends on the constant parameters $K_a$, $K_b$, $\beta$ and the bias current $I$. The other part is a varying term (Eqn. (7)) which is a function of the input signal current, i.e.,

$$\delta_{AC} = f(i)$$

(8)