The microelectronics industry is deeply interested in developing new methods for the reduction of power consumption in digital logic. An innovative solution to the problem is based on thermodynamic reversibility [1–3]. This strategy is implemented in adiabatic logic gates using pulsed power delivery. With rising supply voltage, such a gate performs logical operations while drawing power from the supply; with falling supply voltage, the power supply receives most of the energy that has been stored in the reactors of the gate during the pulse-rise period. Thus, information is produced at the former phase of clock cycle and is deleted at the latter.

Although it is not feasible to completely eliminate dissipation, this can be reduced to any desired extent by decreasing the rate of change of supply voltage, sacrificing the rate with which information is produced. The adiabatic logic in which dissipation is only due to non-zero rate of change of supply voltage and can be made as low as desired is called asymptotically adiabatic logic.

Valiev and Starosel’skii [4] have shown that such logic gates must be as follows:

(i) A gate has three states: a zero state 0, a unity state 1, and a released state \( R \), the third one corresponding to the minimum output energy.

(ii) The input of a gate is set only when the gate is in the \( R \) state.

(iii) An input signal remains at the same logic level over the whole clock cycle of the gate.

(iv) In a gate, every transistor may go to the on state only at zero drain–source voltage.

(v) In a system of gates, there are no feedback loops of feedback factor larger than the critical level inside every gate and between the gates.

Ideally, power consumption must be zero when the gate is in a quiescent state. In reality, spurious currents represent a lower limit of power consumption.

It is commonly accepted that

\[
W \propto T^{-1},
\]

where \( W \) is the energy dissipation per clock cycle and \( T \) is the length of a supply-pulse edge [1, 5, 6].

Quasi-adiabatic gates are the best understood type of adiabatic gate. However, they implement thermodynamic reversibility only to some extent. A review and a categorization of quasi-adiabatic gates were given by Starosel’skii [7].

With quasi-adiabatic logic, the lowest power consumption is offered by 2n–2n2p static gates [8] and by dynamic ones known as efficient charge-recovery logic (ECRL) [9], which are built in the complementary metal–oxide–semiconductor (CMOS) technology. These gates have three states owing to simultaneous use of true and inverted signals. On the other hand, the input signal is lost during the pulse-fall period of supply voltage, and the rest of the five conditions are not satisfied at all. Accordingly, the minimum energy dissipation per clock cycle is

\[
W_{\text{min}} = CV_t^2,
\]

where

\[
V_t = V_{tn} = -V_{tp} > 0
\]

is the absolute value of the threshold voltages \( V_{tn} \) and \( V_{tp} \) for the n- and p-channel transistors, respectively, and \( C \) is the total capacitance of the logic gate [7].

The power consumption of the 2n–2n2p and the ECRL gate was investigated in our previous study [10]. It has been established that

\[
W(T, C) \sim T^{-\alpha}C^1 + \alpha
\]

as \( T \) tends to zero (\( W \gg W_{\text{min}} \)), where \( \alpha = 3/4 \); theoretically, \( \alpha = 1 \) at most. It was also shown that \( \alpha < 1 \) is due to the nonlinear behavior of the transistor channel resistance through which the capacitors are charged and discharged.
This paper reports a computer-simulation study of power consumption in asymptotically adiabatic logic gates of the type 1n–1p (Fig. 1a), whose configuration is identical to conventional CMOS static gates [5]. The 0, 1, and $R$ states correspond to a positive, a negative, and zero output voltages, respectively; they are provided by split-level supply (the $R$ state corresponds to zero supply voltage). Conditions (ii) and (iii) are fulfilled by means of nested supply pulses (Fig. 1c).

Another reason for taking the 1n–1p gate is that it allows us to estimate the increase in dissipation due to violation of any single condition from the above list.

The characteristics of the 1n–1p gate will be compared with the results for 2n–2n2p and ECRL logic.

In a system of logic gates, these should be grouped in blocks such that any $i$th block is driven by its own supply voltage pulse $\phi_i$, as in Fig. 1b.

Let $T_{\text{clk}}$ be the clock period. For an $i$th block, every clock cycle consists of four phases, whose respective lengths are denoted $T_1, T_{2i}, T_3,$ and $T_{4i}$ (Fig. 1c). Phase 1 is activation. As the supply voltage varies from 0 to $V_{dd}/2$, the logic gates produce information, generating the output signal $V_{i0} = -V_{dd}/2$ or $V_{i1} = +V_{dd}/2$, while the capacitors accumulate energy from the power supply. Phase 2 is retention, the supply voltage being kept constant. Phase 3 is deactivation, during which the energy that has been accumulated is transferred to the power supply, the supply voltage returning to zero. Phase 4 is a pause, the block being in the $R$ state. If $T_1 = T_3 = T$, then

$$T_{\text{clk}} = 2T + T_{2i} + T_{4i},$$

Condition (iii) is fulfilled if

$$\delta = (T_{2i} - T_{2i})/2T = \Delta T/T \geq 1,$$  \hspace{1cm} (4)